AMENDMENTS TO THE SPECIFICATION

Please replace **Paragraph 9** (page 3, lines 27-29) with the following paragraph:

- the first source produces a first PTAT (Proportional To the Absolute Temperature) current [[( )]]; and

Please replace **Paragraph 42** (page 8, lines 6-8) with the following paragraph:

the output from the operational amplifier being connected to each of the gates [[grids]] of the first, second and third field effect transistors.

Please replace **Paragraph 49** (page 8, lines 25-27) with the following paragraph:

According to one particular ~~particularly~~ characteristic, the voltage source is remarkable in that the second current generation means comprise:

Please replace **Paragraph 58** (page 9, lines 20-22) with the following paragraph:

the output from the operational amplifier being connected to each of the gates [[grids]] of the fourth and fifth field effect transistors.

Please replace **Paragraph 63** (page 10, lines 7-13) with the following paragraph:

According to one particular characteristic, the voltage source is remarkable in that the [[start]] starting means comprise sixth, seventh and eighth field effect transistors, the gate [[grid]] of each of the transistors being powered by the starter voltage and the source of each of the transistors being powered by a power supply voltage from the voltage source;

Please replace **Paragraph 140** (page 18, lines 10-12) with the following paragraph:

- the gates [[grids]] of transistors M1, M2 and M3 are connected to the output from the operational amplifier A1.

Please replace **Paragraph 142** (page 18, lines 18-28) with the following paragraph:

According to techniques known to those skilled in the art, the current passing through a MOS FET transistor is proportional to the width of the gate [[grid]] of the device. The ratio between the current I1 and the current I2 is thus determined by the ratio of the dimensions of the gates [[grids]] of the MOS transistors M1 and M2; similarly, the ratio between the current I1 and the current I3 is determined by the ratio of the dimensions of the gates [[grids]] of the MOS transistors M1 and M3. The widths of the gates [[grids]] of the MOS transistors M1, M2 and M3 are the same. Thus, for example:

Please replace **Paragraph 146** (page 19, lines 7-14) with the following paragraph:

The gates [[grids]] of MOS transistors M1, M2 and M3 are electrically coupled to the voltage comparison at node N6, generated by amplifier A1. Since the voltage at node N6 is supplied by amplifier A1, the [[grid]] gate-source voltages of MOS transistors M1, M2 and M3 are approximately equal and the MOS transistors M1, M2 and M3 operate at or close to a saturation region during operation of the voltage source 104.

Please replace **Paragraph 176** (page 22, lines 23-26) with the following paragraph:

The MOS transistors M4 and M5 are coupled so as to form the second current mirror 201, the source and gate [[grid]] of the transistor M5 being connected to the source and gate [[grid]] of the transistor M4 respectively:

Please replace **Paragraphs 180-181** (page 23, lines 6-14) with the following paragraphs:

- the gates [[grids]] of transistors M4 and M5 are connected to the output from the operational amplifier A2.

The ratio between the current I3 and the current I5 is determined by the ratio of the dimensions of the gates [[grids]] of MOS transistors M4 and M5. The widths of the gates [[grids]] of MOS transistors M4 and M5 are exactly the same such that the current I5 in transistor M4 is identical to the current I3 in transistor M5.

Please replace **Paragraph 185** (page 23, lines 20-27) with the following paragraph:

The gates [[grids]] of MOS transistors M4 and M5 are electrically coupled to the voltage comparison at node N4 output by amplifier A2. The voltage at node N4 is supplied by amplifier A2, therefore the [[grid]] gate-source voltages of MOS transistors M4 and M5 are approximately equal and the MOS transistors M4 and M5 operate at or close to a saturation region during operation of the voltage source 104.

Please replace **Paragraph 192** (page 24, lines 16-17) with the following paragraph:

- the output from amplifier A2 is connected to the gate [[grid]] of transistor M5 through a node N4; and

Please replace **Paragraph 204** (page 25, lines 26-28) with the following paragraph:

- the width W of the gate [[grid]] of transistors M1, M2, M3, M4 and M5 is equal to 120 μm and the gate [[grid]] length L is equal to 40 μm.

Please replace **Paragraphs 214-217** (page 27, lines 1-13) with the following paragraphs:

The gate [[grid]] of each transistor MPB0, MPB1 and MPB2, and the drain of transistor MNB2 are connected to bias circuit 100.

The drain of transistor MPB1 is connected to the drain of each of transistors MNST1 and MNB1 and to the gate [[grid]] of each of transistors MNB1 and MNB2. The drain of transistor MPB1 outputs a current iBIAS;

The drain of transistor MPB0 is connected to one of the terminals of the capacitor CST (the other terminal of this element being connected to the ground 11) and to the gate [[grid]] of each of the transistors I31 and I32.

The drain of transistor I32 is connected to the gate [[grid]] of transistor MNDT1 and to the drain of transistor I31.

Please replace **Paragraph 225** (page 28, lines 1-4) with the following paragraph:

- parameters L_NB1 and L_NB2 represent the gate [[grid]] lengths (in other words the distance between the drain and the source) of the transistors MNB1 and MNB2 respectively; and

Please replace **Paragraphs 231-234** (page 28, lines 18-28) with the following paragraphs:

- the width of the gate [[grid]] of transistors MPB0, MPB1 and MPB2 is equal to 10 μm and their length is equal to 1.26 μm;
- the width of the gate [[grid]] of transistors I31 and I32 is equal to 2.5 μm and 5 μm respectively, and their length is equal to 0.35 μm;
- the width of the gate [[grid]] of transistor MNST1 is equal to 4.9 μm and its length is equal to 0.35 μm;
- the width and length of the gate [[grid]] of each transistor MNB1 and MNB2 are equal to 26 μm and 1.2 μm respectively.

Please replace **Paragraph 240** (page 29, lines 11-16) with the following paragraph:

Transistors M6, M7 and M8 enable satisfactory startup of the voltage source 104. For example, the width of the gate [[grid]] of transistors M6, M7 and M8 is equal to 10 µm and their length is equal to 1.26 µm, these dimensions being identical to the dimensions of transistors MPB0, MPB1 and MPB2.

Please replace **Paragraph 242** (page 29, lines 19-20) with the following paragraph:

The gate [[grid]] of each of the transistors M6, M7 and M8 is connected to the bias voltage vbias.

Please replace **Paragraph 271** (page 32, lines 2-7) with the following paragraph:

The PTAT current source 501 is similar to the source 101 previously illustrated with reference to FIGS. 2 and 4, except for the current mirror 200 that also comprises a transistor M33 for which the source and the gate [[grid]] are connected in parallel to the source and gate [[grid]] respectively of transistor M3.

Please replace **Paragraph 272** (page 32, lines 8-13) with the following paragraph:

The surface area of the gate [[grid]] of transistor M33 is not the same as the surface area of the gate [[grid]] of transistor M3. Thus, the currents I4 and I6 output by transistors M3 and M33 respectively are different. If the gate [[grid]] of M33 is larger than the gate [[grid]] of M3, the current I6 will vary with a positive temperature coefficient.

Please replace **Paragraphs 276-276** (page 32, lines 17-26) with the following paragraphs:

The CPTAT current source 502 is similar to the source 102 previously illustrated with reference to FIGS. 2 and 4, except for the current mirror 201 that also comprises a transistor M44 for which the source and the gate [[grid]] are connected in parallel to the source and the gate [[grid]] respectively of transistor M4.

Transistors M4 and M44 have identical gate [[grid]] widths and lengths. Thus, the current I7 output by transistor M44 is identical to the current I5 output by transistor M4.